CLAIMS

1. A memory cell having a source (201, 502), a channel (212, 503) formed over the source, a drain (203, 714) formed over the channel, and a substantially vertical select gate (205) formed in a trench generally adjacent to the channel, the memory cell further characterized by:

a substantially horizontal floating gate formed over at least a portion of the drain, wherein the horizontal floating gate is defined by a sublithographic feature dimension, the channel is defined substantially vertically between the source and drain, and the feature size of the memory cell is not greater than $2F^2$.

2. The memory cell of claim 1, wherein the source is a buried layer.

3. The memory cell of claim 1, wherein the horizontal floating gate is a sublithographic floating gate defined by a spacer.

4. The memory cell of claim 1, wherein the horizontal floating gate is a self aligned floating gate.

5. The memory cell of claim 1 wherein:

the substantially vertical select gate is formed substantially perpendicular to the horizontal floating gate.

6. The memory cell of claim 5, wherein the memory cell has a minimum feature size corresponding to the horizontal floating gate and the vertical select gate.

7. The memory cell of claim 1, wherein the memory cell has a feature size not greater than $2F^2$ defined by a first dimension of F which is half of a digitline pitch, and a feature size of 2F in a second dimension which is a wordline pitch.

8. The memory cell of claim 1, wherein:

the source is defined by a first n-type layer that is formed over a substrate;

the substantially vertical channel is formed in a p-type layer that is formed over the first n-type layer; and

the drain is formed in a second n-type layer that is formed over the p-type layer.

9. The memory cell of claim 8, further comprising:

a tunnel oxide layer formed over the substrate;

a first poly layer formed over portions of tunnel oxide layer defining the sublithographic horizontal floating gates;

trenches formed in the p-type layer; and

a select gate formed on sidewalls of the trenches.

10. The memory cell of claim 8, further comprising:

a conductive layer formed over at least a portion of the second n-type layer;

a first spacer formed on the conductive layer;

a tunnel oxide layer formed over at least a portion of the substrate;

a polysilicon layer formed on the tunnel oxide layer; and

an oxide layer formed on the polysilicon layer.

11. The memory device of claim 8, further comprising

digitlines and wordlines formed over the memory device.

12. The memory device of claim 11, wherein the wordlines are above the digitlines.

13. The memory device according to claim 11, wherein the digitlines comprise:

A TiSi layer formed on the substrate;

a TiN layer formed on the TiSi layer;

a tungsten bitline formed on the TiN layer.

14. A method of forming a memory cell having a square feature size of less than $4F^2$ comprising:

providing a substrate;

forming a source over said substrate;

forming a substantially vertical channel over the source;

forming a drain over the vertical channel; and

forming a substantially horizontal floating gate over at least a portion of the drain such that the floating gate is defined by a sublithographic feature dimension, wherein the overall feature size of the memory cell is not greater than $2F^2$.

15. The method of claim 14, wherein the horizontal floating gate is provided by a sublithographic feature dimension comprising:

forming a first oxide layer over the substrate;

forming a poly layer over the first oxide layer;

forming a second oxide layer over the poly layer; and

using a removable spacer to define the floating gate sublithographically.

16. The method of claim 14, wherein forming a source over the substrate comprises forming a buried source over the substrate.

17. The method of claim 16, wherein forming the buried source comprises:

providing a wafer having a substrate;

covering a periphery of a wafer using an array mask;

doping source areas with a dopant; and

performing an epitaxial deposition to a determined thickness to form a channel, wherein the thickness determines a channel length.

18. The method of claim 14, wherein said memory cell is limited being not greater than $2F^2$ in size by forming the memory cell to have a feature size of 1F in a first dimension defined by one half of a digitline pitch, and a feature size of 2F in a second dimension defined by a wordline pitch.

19. The method of claim 14, wherein forming the substantially vertical channel over the source comprises:

forming a source in a first n-type layer; and

forming a first p-type layer over the first n-type layer.

20. The method according to claim 19, wherein the p-type layer is formed using epitaxial deposition.

21. The method of claim 14, further comprising:

forming a first n-type layer;

forming the source in the first n-type layer;

forming the substantially vertical channel in a p-type material;

performing a cell implant;

forming a tunnel oxide layer over the substrate;

forming a first poly layer over the tunnel oxide layer;

forming a nitride layer over the first poly layer;

patterning wordlines into the memory device;

forming STI areas in the memory device;

removing the nitride layer; and

forming an oxide nitride oxide layer over a surface of the memory device.

22. The method of claim 21, wherein forming STI areas in the memory device further comprises etching the nitride layer and etching the first poly layer.

23. The method of claim 21, wherein forming STI areas in the memory device further comprises depositing an STI oxide over the STI areas and filling the STI areas with a field oxide.

24. The method of claim 21, further comprising:

polishing a surface of the memory device using chemical mechanical polishing to make the surface planar.

25. The method of claim 21, further comprising:

forming a STI area and a self aligned floating gate;

depositing a BPSG layer over the substrate;

depositing a hardmask layer over the BPSG layer;

patterning active areas to form an trench;

forming first spacers along sidewalls of the trench;

forming a drain in the trench; and

forming a wordline over the drain.

26. The method of claim 25, further comprising performing rapid thermal processing on the memory device and polishing the surface of the memory device prior to depositing the hardmask layer.

27. The method of claim 25, wherein patterning active areas further comprises etching through the hardmask layer, the BPSG layer, an oxide nitride oxide layer and a first poly layer.

28. The method of claim 25, wherein forming first spacers comprises depositing a first spacer layer and etching the first spacer layer thereby leaving the first spacers along the sidewalls of the trench.

29. The method of claim 25, further comprising:
forming a TiN layer over the trench; and
forming a TiSi layer over the trench.

30. The method of claim 25, further comprising:
performing a rapid thermal process on the memory device prior to forming a wordline.

31. The method of claim 25, wherein forming a wordline comprises:
depositing a wordline layer over the trench;
polishing the wordline layer such that the wordline layer is planar to the hardmask layer; and
removing a portion of the wordline layer such that a lower portion of the wordline layer remains.

32. The method of claim 31, wherein removing a portion of the wordline layer comprises removing substantially half of the wordline layer.

33. The method of claim 25, further comprising depositing a second spacers over the wordline.

34. The method of claim 14, further comprising:

forming a select transistor oxide layer over the trench;

forming a poly layer over the surface of the memory device;

forming a conductive layer over the poly layer; and

patterning the poly layer and the conductive layer.

35. The method of claim 14, wherein forming the select gate comprises:

forming an oxide layer in the select trench; and

filling the select trench with polysilicon.

36. The method according to claim 14, further comprising:

forming digitlines and wordlines over the substrate.

37. The method according to claim 36, further comprising forming the wordlines above the digitlines.

38. The method according to claim 36, further comprising forming the digitlines above at least a portion of the drain.

39. The method according to claim 38, wherein said bitline comprises a tungsten layer, the method further comprising:

forming a layer of TiSi over the substrate and under the bitline;

forming a layer of TiN between the TiSi and bitline; and

forming the bitline from tungsten over the TiN.

40. The method according to claim 39, further comprising forming a spacer between the digitlines and the wordlines.